**CDA 4213/CIS 6930 CMOS VLSI**

**Fall 2019**

**Final Project**

**Due date(s)**

**Partial Design Report:**

Week of 18th November

**Final Design Report:**

Monday, 9th December

|  |  |
| --- | --- |
| Today’s Date: |  |
| Your Team Name: | *(Choose an acronym or a name for your team. Be creative!)* |
| Team Members: |  |
| Work Distribution | Explain in detail, who has done what. Each team member’s grade will be based on their overall contribution.  1)  2)  3) |
| No. of Hours Spent: |  |
| Exercise Difficulty:  (Easy, Average, Hard) |  |
| Any Feedback: |  |

1. **(10 pts)** Proposed Design – Bit slice design

(a) List all module bit-slices you have used for your design.

(b) For each bit slice, show the gate-level design and layout design. For layout, include the snapshot from Cadence Virtuoso. If you have used any other blocks, include them as well.

1. Full Adder:
2. Full Adder with AND gate:
3. Registers (Inputs and Output):
4. Ring Oscillator (If used):
5. **(15 pts.)** Show the layout of your multiplier with the registers (outside the padframe). Explain the design and functionality of your multiplier.

1. **(25pts)** Simulation Results (without padframe):
2. (5 pts total) Individual cells:
3. Full Adder:
4. Full Adder with AND gate:
5. Registers (Test Mode):
6. Ring Oscillator (If used):
7. (20 pts) The final multiplier:
8. **(10 pts.)** Layout of the final design (with padframe):
9. **(20 pts)** Simulation waveforms for the final design (with padframe):